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Structure and Process for Packaging Back-to-Back Chips

Abstract

A packaging structure for back-to-back chips, which includes: a substrate, a first chip, a second chip, and an encapsulation. Wherein, the first chip has an active side and an inactive side, and the active side of the first chip is connected to the substrate by an adhesion layer and conducted electrically with the substrate by wire-bonding. The second chip has an active side that is also conducted electrically with the substrate by wire-bonding and an inactive side that is connected to the inactive side of the first chip by another adhesion layer. The encapsulation covers both the first chip and the second chip for protecting the back-to-back packaging structure.